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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,091	06/28/2002	Gilbert Wolrich	10559-310US1	7309

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,091	WOLRICH ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/13/04,12/05/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

09/07/06

1. Claims 1-8,10-21 are presented for examination. Claims 9 and 22 have been canceled.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1, 21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

3. As to claims 1, 21, Claims 1, 21 are not limited to tangible embodiments. In view of applicant's disclosure, specification page (2), line (3-15), the method or the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., (hardware based processor)) and intangible embodiments (e.g., (internet). Although the claim recite the instructions cause the access of absolutely address and relatively address, based on broadest interpretation, it is read as intended use , not a positive limitation. The focus is not on the steps or feature taken to achieve the final result which is useful, tangible, and concrete, but rather the final result achieved which is useful, tangible, and concrete (see page 20, 101 Interim Guidelines published at uspto.gov) . No final result which is useful, tangible, and concrete can be found in the claims. Therefore, it is directed non-statutory subject matter.

As to claim 12, claim 12 is not being rejected under "101: because it has the positive recitation of hardware based processor and the arithmetic unit (see claim 12, line 1,5). However, examiner would like to suggest the change of the language : "control logic" into "control logic circuit", or the like, to avoid possible broader interpretation of the claim.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Panwar et al. (5,870,597).

5. As to clam 1, Panwar disclosed maintaining execution thread in a parallel multithreaded processor (see consistent implementation of multithreaded processor 102 in col.6, lines 40-44) comprising accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively

addressable windows of registers that are relatively addressable per thread (see the registers sets organized into register windows in col.2, lines 40-65, see the window pointer CWP for the relative addressable registers, see also the movable windows within the register file in col.7, lines 40-67, col.8, lines 1-5).

wherein accessing absolutely any one of the relatively(see register sepecifier) and absolutely addressable (see physical address) registers comprises providing an exact address of the register. the exact address specified in an instruction associated with the thread (see the five bit register addresses encoded in an instruction word in col.2, lines 53-67, col.3, lines 1-13).

6. As to claim 2, Panwar also included same relative register address (window pointer) but access different banks od registers (register sets, see col.2, lines 40-65).

7. As to claim 3, Panwar's elative address also divided the register banks (register sets) into windows across address width of general purpose registers (see the general purpose registers in col.2, lines 40-65).

8. As to claim 4, Panwar also accessed any of the windows with a starting point (see the manipulation of the window position and the window permitted the movable subsets of registers in col.2, lines 40-65, see also the logical and index address in col.2, lines 67-68, col.3, lines 1-6).

9. As to claim 5, Panwar also organized the register sets in to windows according to the number of threads (see the 3 register windows per one instruction bundle in fig.5, col.9, lines 5-33, see also multithreaded in col.2, lines 40-65).

10. As to claim 6, Panwar also allowed different windows perform different functions (see different processes call their own windows in col.7, lines 39-46).

11. As to claim 7, Panwar also taught dual port memory (see the multiported memory in col.1, lines 44-45).

12. As to claim 8, Panwar also allowed any starting point (see the manipulation of the window position and the window permitted the movable subsets of registers in col.2, lines 40-65, see also the logical address in col.2, lines 67-68, col.3, lines 1-6).

13. As to claim 9, Panwar also included absolute address (see the physical addresses in col.2, lines 53-65).

14. As to claim 10, Panwar also included source field and destination field (see destination and source in col.2, lines 66-67, col.6, lines 1-5).

15. As to claim 11 , see offset in col.7, lines 54-56).

16. As to claim 12, Panwar taught at least a hardware based multi-threaded processor (see the consistent use of multithreaded processor in col.6, lines 40-44) Comprising :

a) control logic (204) (206) including context event switching logic, the context switching logic arbitrating access to a microengine for a plurality of executable threads (see the functions performed by scheduling units 204 and 206 in col.6, lines 27-58, see also the Save and Restore of the registers in col.7, lines 62-67, col.8, lines 1-41);

b) an arithmetic logic unit to process data for executing threads (see either 208 integer or 210 floating point , col.6, lines 31-33)., and

c) a register set that is organized into a plurality of relatively addressable windows of

registers that are relatively addressable executable thread (see col.7, lines 40-46).

17. As to claim 13, Panwar also included :

an instruction decoder (see instruction decode in col.6, lines 63-64, col.7, lines 1 1-13), and program counter units to track executing threads (see the redirection of execution of multiple treaded operations by the dispatch unit 206 in col.6, lines 27-44, see also instruction identified by controller 502 in col.9, lines 54-60, see also a branch identifier in col .1 1 , lines 29-33).

18. As to claim 14, Panwar also included program counters units are maintained in hardware (see the dispatcher 206 and controller 502).

As to claim 15, Panwar also taught register banks (sets) organized into windows across an address width of the general purpose register set with each window relatively accessible by a corresponding thread (see general purpose registers in col.2, lines 39-65, see the register windows movable by a process or program in col.7, lines 40-47, see the logical and index addresses in col.2, lines 62-67, col.3, lines 1-5 for relative addresses).

19. As to claim 16, Panwar also taught relative addressing allows access to any of the registers relative to the starting point of a window of registers (see the manipulation of the window position and the window permitted the movable subsets of registers in col.2, lines 40-65, see also the logical address in col.2, lines 67-68, col.3, lines 1-6). .

20. As to claim 17, Panwar also taught number of windows of the register set is according to the number of threads that execute in the processor (see the 3 register

windows per one instruction bundle in fig.5, col.9, lines 5-33, see also multithreaded in col.2, lines 40-65).

21. As to claim 18, Panwar also taught relative addressing allow the multiple threads to use the same control store and locations while allowing access to different windows of register and perform different functions (see different processes with their own windows in col.7, lines 39-47).

22. As to claim 19, Panwar also taught dual ported memory (see col.1, lines 44-45).

23. As to claim 20, Panwar also taught a micro preprogrammed processor unit (see program running on microprocessor in col.2, lines 30-41).

24. As to claim 21, Panwar taught a computer program product residing on a computer readable medium (see fig.1, col.5, lines 120) for managing execution of multiple threads (see multiple treaded operation in col.6, lines 36-44) in a multithreaded processor comprising instructions causing a processor to: access, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively addressable windows of registers that are relatively addressable per thread (see movable register windows col.2, lines 40-65, coll7, lines 40-46, see also the window pointers).

25. As to claim 21, Panwar also included absolutely addressable registers where any one of the absolutely addressable registers may be accessed by any of the threads by providing the exact address of the register (see the physical address of the registers in col.9, lines 50-53).

26. Claim 1-6,8,10-18,20,21 are rejected under 35 U.S.C. 102(b) as being anticipated by Sollars (5,900,025) .

27. As to claims 1,5,12,20, 21, Sollars disclosed maintaining execution thread in a parallel multithreaded processor (see the concurrent execution of eight threads in col.2, lines 1-14) comprising :

a) accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively addressable windows of registers that are relatively addressable per thread (see the virtually/physically addressable operand register sets in col.5, lines 20-31, see also the partitioned control register subsets in col.5, lines 32-54, col.6, lines 36-67, col.7, lines 1-7, col.7, lines 38-67, col.8, lines 1-11, see also fig.3 and fig.4 for corresponding virtual/physical addressable registers sets, see how register file [register set] organized into register sets [102][104][106] [register windows], see also how the register set 102 further organized into subsets 108).

wherein accessing absolutely any one of the relatively (see virtually addressable) and absolutely addressable (see physically addressable) registers comprised providing an exact address of the register (see register addresses in col.8, line5-11) , the exact address specified in an instruction associated with the thread (see the operand register sets accessible by the instruction in col.5, lines 25-26, see also the control registers accessible by instruction in col.5, lines 48-51).

28. As to the context switching logic in claim 12, see context switching in col.1, lines 19-28.

29. As to the arithmetic unit, see arithmetic unit in fig.18a,b.

30. As to claim 2, Sollars also included access of the different windows (see the different number of the dynamically associated thread 106 in col.7, lines 25-37).

31. As to claim 3, Sollars partitioned register file was general purpose because it was used for conventional functions (see col.5, lines 20-35).

32. As to claims 4,8, 11, Sollar also included starting point of the window of registers (see the address of the base register set in col.8, lines 5-11).

33. As to claim 6, 18, see single context multiple threads in col.7, lines 9-23.

34. As to clam 10, since Sollars also taught his registers sets are operand registers , therefore, the source and destination must be included, such as source opened or destination operand.

35. As to claim 13, see IFU for decoding and executing in col.6, lines 16-34.

36. AS to claim 14, see fig.6 program counter.

37. As to claims 15,16, see relative address to the base address in col.8, lines 5-11.

38. As to claim 17, since Solars already taught that his context registers having different number of dynamically associated thread level control register sets drawn t form a common pool of thread level control sets and can allocated and deallocated

(see col.7, lines 25-37), Sollars should have the number of register windows according to the number of threads.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claim 7,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solars (5,900,025) in view of Panwar (5,870,597) .

40. As to claims 7,19, Sollars did not specifically show the dual port as claimed. however, Panwar taught dual port memory (see the multiported memory in col.1, lines 44-45). It would have been obvious to one of ordinary skill in the art to sue Panwar in Solars for including dual port as clamed because the use of Panwar could provide Sollars the ability to accept the multiple of data sets , thereby increasing the data bandwidth of the system, and Sollars did teach the partitioning of the register set (see col.5, lines 55-65), which was the suggestion of the need for providing more than one port of the registers file in order to accommodate the multiple register file subsets, in doing so, provided a motivation.

41. The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

a) Shaylor (6,408,325) is cited for the teaching of the register sets in windows with the context switching technique (see col.3, lines 1-17, col.4, lines 29-51 , see col.5, lines 32-43).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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